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EXAMINER	
FOTAKIS, ARISTOCRATIS	
ART UNIT	**PAPER NUMBER**
2611	

NOTIFICATION DATE	DELIVERY MODE
06/04/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@ti.com
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Office Action Summary	Application No.	Applicant(s)	
	10/766,448	SUISSA ET AL.	
	Examiner	Art Unit	
	Aristocratis Fotakis	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 3, 5, 8 - 11, 13 - 14, 16 - 17* is/are rejected.

7)☒ Claim(s) *4, 6 –7, 12, 15 and 18 – 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1 – 3 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 2, 5 and 9 of U.S. Patent No. 6,882,208 in view of Koomullil et al (US Pub 20030133518).

Re claim 1, *claims 2 and 9* of patent (6,882,208) recite of a method of frequency offset compensation, said method comprising the steps of: first determining a current maximum peak value of said input signal; second determining a current minimum peak value of said input signal; calculating an average of said current maximum peak value and said current minimum peak value to yield a DC offset estimate; and subtracting said DC offset estimate from said input signal to yield a frequency compensated output signal (Col 10, Lines 50 – 59 and Col 11, Lines 28 – 30).

However, *claims 2 and 9* of patent (6,882,208) do not specifically recite of receiving an input signal wherein frequency offsets have been translated to DC offsets.

Koomullil teaches of a wireless communication system and methods for estimating and correcting DC offset in the presence of carrier frequency offset (Paragraph 0003). The IF signal is filtered and amplified before being converted to the baseband. Conversion to the baseband generally involves mixing the IF signal with the output of a second local oscillator operating at the intermediate frequency (end of Paragraph 0005). Because zero-IF receivers can operate at lower power and be more easily integrated into monolithic systems than heterodyne receivers, such receivers are recognized as potentially very useful for applications where low cost, low power consumption, and small size are important, such as various wireless mobile handheld devices (end of paragraph 0006).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have translated the frequency offsets to DC offsets for a zero-IF receiver for the benefit of low cost, low power consumption, and small size.

Re claim 2, *claim 2* of patent (6,882,208) recite of determining said current maximum peak value comprising the steps of: comparing said input signal with a previous maximum peak value; if said input signal is greater than said previous maximum peak value, adding said current maximum peak value to a first difference between said input signal and said previous maximum peak value, said first difference multiplied by a maximum charge coefficient to yield said current maximum peak value; and if said input signal is not greater than said previous maximum peak value, subtracting a second difference between said current maximum peak value and said input signal multiplied by a maximum discharge coefficient from said previous maximum peak value to yield said current maximum peak value (Col 10, Lines 60 – 67 to Col 11, Lines 1 – 8).

Re claim 3, *claim 5* of patent (6,882,208) recite of the step of generating said maximum charge coefficient and said maximum discharge coefficient in accordance with the occurrence of a specific event (Col 11, Lines 14 – 17).

Claims 1 and 5 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 10 of U.S. Patent No. 6,882,208 in view of Koomullil et al (US Pub 20030133518).

Re claim 1, *claim 10* of patent (6,882,208) recite of a method of frequency offset compensation, said method comprising the steps of: first determining a current maximum peak value of said input signal; second determining a current minimum peak value of said input signal; calculating an average of said current maximum peak value and said current minimum peak value to yield a DC offset estimate (Col 11, Lines 31 – 44).

However, *claim 10* of patent (6,882,208) do not specifically recite of receiving an input signal wherein frequency offsets have been translated to DC offsets and subtracting said DC offset estimate from said input signal to yield a frequency compensated output signal.

Koomullil teaches of a wireless communication system and methods for estimating and correcting DC offset in the presence of carrier frequency offset (Paragraph 0003). The IF signal is filtered and amplified before being converted to the baseband. Conversion to the baseband generally involves mixing the IF signal with the output of a second local oscillator operating at the intermediate frequency (end of Paragraph 0005). Because zero-IF receivers can operate at lower power and be more easily integrated into monolithic systems than heterodyne receivers, such receivers are recognized as

potentially very useful for applications where low cost, low power consumption, and small size are important, such as various wireless mobile handheld devices (end of paragraph 0006). In a receiver for an RF communication system, a DC offset compensation circuit includes a subtraction circuit, a phase correction circuit, a first multiplier circuit, an averaging circuit, an adjustment circuit, and an updating circuit. The subtraction circuit is configured to subtract a stored DC offset value from a received signal, thereby producing a first corrected signal (Paragraph 0014).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have translated the frequency offsets to DC offsets for a zero-IF receiver for the benefit of low cost, low power consumption, and small size and subtracting the DC offset estimate from the input signal to yield a frequency compensated output signal to avoid errors in the reconstruction of the transmitted signal.

Re claim 5, *claim 10* of patent (6,882,208) recite of the step of determining said current minimum peak value comprises the steps of: comparing said input signal with a previous minimum peak value; if said input signal is not greater than said previous maximum peak value, subtracting a first difference between said current minimum peak value and said input signal, said first difference multiplied by a minimum discharge coefficient and subtracted from said previous minimum peak value to yield said current minimum peak value; and if said input signal is greater than said previous minimum

peak value, adding said current minimum peak value to a second difference between said input signal and said previous minimum peak value, said second difference multiplied by a minimum charge coefficient to yield said current minimum peak value (Col 11, Lines 40 – 57).

Claims 9 - 11 and 13 – 14 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 12, 15 - 16 and 19 of U.S. Patent No. 6,882,208 in view of Koomullil et al (US Pub 20030133518).

Re claim 9, *claims 12 and 16* of patent (6,882,208) recites of an apparatus for frequency offset compensation, comprising: first means for receiving an input signal wherein frequency offsets have been translated to DC offsets; second means for determining a current maximum peak value of said input signal; third means for determining a current minimum peak value of said input signal; fourth means for calculating an average of said current maximum peak value and said current minimum peak value to yield a DC offset estimate; and fifth means for subtracting said DC offset estimate from said input signal to yield a frequency compensated output signal (Col 12, Lines 1 – 9 and Lines 36 - 44).

However, *claims 12 and 16* of patent (6,882,208) do not specifically recite of receiving an input signal wherein frequency offsets have been translated to DC offsets

and subtracting said DC offset estimate from said input signal to yield a frequency compensated output signal.

Koomullil teaches of a wireless communication system and methods for estimating and correcting DC offset in the presence of carrier frequency offset (Paragraph 0003). The IF signal is filtered and amplified before being converted to the baseband. Conversion to the baseband generally involves mixing the IF signal with the output of a second local oscillator operating at the intermediate frequency (end of Paragraph 0005). Because zero-IF receivers can operate at lower power and be more easily integrated into monolithic systems than heterodyne receivers, such receivers are recognized as potentially very useful for applications where low cost, low power consumption, and small size are important, such as various wireless mobile handheld devices (end of paragraph 0006). In a receiver for an RF communication system, a DC offset compensation circuit includes a subtraction circuit, a phase correction circuit, a first multiplier circuit, an averaging circuit, an adjustment circuit, and an updating circuit. The subtraction circuit is configured to subtract a stored DC offset value from a received signal, thereby producing a first corrected signal (Paragraph 0014).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have translated the frequency offsets to DC offsets for a zero-IF receiver for the benefit of low cost, low power consumption, and small size and subtracting the DC offset estimate from the input signal to yield a frequency compensated output signal to avoid errors in the reconstruction of the transmitted signal.

Re claim 10, *claim 12* of patent (6,882,208) recites of the second means for determining said current maximum peak value comprises: means for comparing said input signal with a previous maximum peak value; means for adding said current maximum peak value to a first difference between said input signal and said previous maximum peak value, said first difference multiplied by a maximum charge coefficient to yield said current maximum peak value if said input signal is greater than said previous maximum peak value; and means for subtracting a second difference between said current maximum peak value and said input signal multiplied by a maximum discharge coefficient from said previous maximum peak value to yield said current maximum peak value if said input signal is not greater than said previous maximum peak value (Col 12, Lines 10 – 25).

Re claim 11, *claim 15* of patent (6,882,208) recites of further comprising gear shift logic means for generating said maximum charge coefficient and said maximum discharge coefficient in accordance with the occurrence of specific events (Col 12, Lines 32 – 35).

Re claim 13, *claim 16* of patent (6,882,208) recites of the third means for determining said current minimum peak value comprises: means for comparing said input signal with a previous minimum peak value; means for subtracting a first difference between said current minimum peak value and said input signal, said first

difference multiplied by a minimum discharge coefficient and subtracted from said previous minimum peak value to yield said current minimum peak value if said input signal is not greater than said previous maximum peak value; and means for adding said current minimum peak value to a second difference between said input signal and said previous minimum peak value, said second difference multiplied by a minimum charge coefficient to yield said current minimum peak value if said input signal is greater than said previous minimum peak value (Col 12, Lines 45 – 61).

Re claim 14, *claim 19* of patent (6,882,208) recites of further comprising gear shift logic means for generating said minimum charge coefficient and said minimum discharge coefficient in accordance with the occurrence of a specific event (Col 13, Lines 1 – 4).

Claim 17 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 20 of U.S. Patent No. 6,882,208 in view of Koomullil et al (US Pub 20030133518).

Re claim 17, *claim 20* of patent (6,882,208) recites of an apparatus for frequency offset compensation, comprising: first means for receiving an input signal; second means for determining a current maximum peak value of said input signal comprising; means for comparing said input signal with a previous maximum peak value; means for

adding said current maximum peak value to a first difference between said input signal and said previous maximum peak value, said first difference multiplied by a maximum charge coefficient to yield said current maximum peak value if said input signal is greater than said previous maximum peak value; means for subtracting a second difference between said current maximum peak value and said input signal multiplied by a maximum discharge coefficient from said previous maximum peak value to yield said current maximum peak value if said input signal is not greater than said previous maximum peak value; third means for determining a current minimum peak value of said input signal comprising; means for comparing said input signal with a previous minimum peak value; means for subtracting a first difference between said current minimum peak value and said input signal, said first difference multiplied by a minimum discharge coefficient and subtracted from said previous minimum peak value to yield said current minimum peak value if said input signal is not greater than said previous maximum peak value; means for adding said current minimum peak value to a second difference between said input signal and said previous minimum peak value, said second difference multiplied by a minimum charge coefficient to yield said current minimum peak value if said input signal is greater than said previous minimum peak value; fourth means for calculating an average of said current maximum peak value and said current minimum peak value to yield a DC offset estimate (Col 13, Lines 5 – 37 to Col 14, Lines 1 – 8).

However, *claim 20* of patent (6,882,208) do not specifically recite of receiving an input signal wherein frequency offsets have been translated to DC offsets and

subtracting said DC offset estimate from said input signal to yield a frequency compensated output signal.

Koomullil teaches of a wireless communication system and methods for estimating and correcting DC offset in the presence of carrier frequency offset (Paragraph 0003). The IF signal is filtered and amplified before being converted to the baseband. Conversion to the baseband generally involves mixing the IF signal with the output of a second local oscillator operating at the intermediate frequency (end of Paragraph 0005). Because zero-IF receivers can operate at lower power and be more easily integrated into monolithic systems than heterodyne receivers, such receivers are recognized as potentially very useful for applications where low cost, low power consumption, and small size are important, such as various wireless mobile handheld devices (end of paragraph 0006). In a receiver for an RF communication system, a DC offset compensation circuit includes a subtraction circuit, a phase correction circuit, a first multiplier circuit, an averaging circuit, an adjustment circuit, and an updating circuit. The subtraction circuit is configured to subtract a stored DC offset value from a received signal, thereby producing a first corrected signal (Paragraph 0014).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have translated the frequency offsets to DC offsets for a zero-IF receiver for the benefit of low cost, low power consumption, and small size and subtracting the DC offset estimate from the input signal to yield a frequency compensated output signal to avoid errors in the reconstruction of the transmitted signal.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Yang et al (US 5,652,541).

Yang teaches of a method of frequency offset compensation, said method comprising the steps of: receiving an input signal wherein frequency offsets have been translated to DC offsets (Fig. 2 and 4) (Col 1, Lines 47 – 52); first determining a current maximum peak value of said input signal (#409, Fig.4, Col 6, Lines 17 – 31); second determining a current minimum peak value of said input signal (#411, Fig.4, Col 6, Lines 17 – 31); calculating an average of said current maximum peak value and said current minimum peak value to yield a DC offset estimate (#405, #407, Fig.4, Col 6, Lines 17 – 31); and subtracting said DC offset estimate from said input signal to yield a frequency compensated output signal (Col 4, Lines 14 – 16).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 8 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang in view of Boccuzzi (US 5,550,868).

Yang discloses all the limitations of claims 1 and 9 except of calculating a moving average.

Boccuzzi teaches of a π/4 delay spread detection and compensation arrangement effectively detecting distortion due to multipath delay spread in a digital channel and compensating for this distortion with minimum circuit complexity. An improvement in the bit error rate performance for a differential detector in the receiver is achieved through use of a detected direct current (DC) component, which is proportional to the amount of multipath delay spread on the digital channel. This DC component is used in the differential detector for compensating for this delay spread (Abstract). The estimated DC offset in the moving average unit (#311, Fig.3) may be obtained in either of two ways--from a moving average filter or a running average filter (Col 7, Lines 9 – 11).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used moving average for a more accurate and stable dc offset estimation.

Allowable Subject Matter

Claims 4, 6 –7, 12, 15 and 18 – 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aristocratis Fotakis whose telephone number is (571) 270-1206. The examiner can normally be reached on Monday - Thursday 7 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AF

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER